AMENDMENT(S) TO THE CLAIMS

1. (currently amended) A memory controller comprising:

refresh logic to refresh memory cells of at least one memory device; and

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells of the at least one memory device, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use;

wherein the refresh logic is configured to omit refreshing of memory cells that are not in use and the memory controller comprises at least part of a device other than the at least one memory device.

2. (previously presented) A memory controller as recited in claim 1, wherein the refresh logic on the memory controller is configured to not refresh the indicated unused groups of memory cells.

3. (previously presented) A memory controller as recited in claim 1, further comprising recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory controller is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

4. (previously presented) A system comprising the memory controller as recited in claim 1, further comprising a plurality of memory devices, which include the at least one memory device, that comprise the groups of memory cells.

5. (previously presented) A system comprising the memory controller as recited in claim 1, the system further comprising a plurality of memory devices that include recent-access flags configured to indicate whether associated sets of the memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

6. (previously presented) A memory controller as recited in claim 1, further comprising:

a cache that is adapted to cache at least some of those memory cells that are indicated by the use registers to be in use and to omit refreshing of the cached memory cells.

7. (previously presented) A memory controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a set of memory cells.

8. (previously presented) A memory controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a row of memory cells.

9. (previously presented) A memory controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a bank of memory cells.

10. (previously presented) A memory controller as recited in claim 1, wherein the use registers comprise bits that each correspond to a page of memory cells.

11. (currently amended) A system comprising:

a plurality of memory devices having memory cells; and

a memory controller on a different device including one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are programmable to indicate whether the corresponding groups of memory cells are in use.

12. (previously presented) A system as recited in claim 11, further comprising:

refresh logic that is configured not to refresh unused memory cells.

13. (previously presented) A system as recited in claim 11, further comprising:

recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated

sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the system is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

14. (previously presented) A system as recited in claim 13, wherein the recent-access flags are part of the plurality of memory devices.

15. (previously presented) A system as recited in claim 13, wherein the recent-access flags are part of the memory controller.

16. (previously presented) A system as recited in claim 11, wherein the memory controller is configured to operate unused memory cells at reduced power.

17. (previously presented) A system as recited in claim 11, further comprising:

a cache that is adapted to cache at least some of those memory cells whose use registers indicate they are not unused;

wherein the memory controller is configured to omit refreshing of the cached memory cells.

18. (previously presented) A system as recited in claim 11, wherein the use registers comprise bits that each correspond to a row of memory cells.

19. (previously presented) A system comprising:

one or more memory devices having dynamically refreshable memory cells;

a memory controller having refresh logic configured to periodically refresh the memory cells of the memory devices;

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use;

wherein the refresh logic is further configured not to refresh memory cells that are not in use; and

recent-access flags associated with the memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the refresh logic is further configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval,

wherein the use registers are not implemented on a same device as the memory cells.

20. (previously presented) A system as recited in claim 19, wherein the recent-access flags are not implemented as part of the memory controller.

21. (previously presented) A system as recited in claim 19, wherein the memory controller is configured to cache at least some of those memory cells that are not indicated by the one or more use registers to be unused; and wherein the refresh logic is further configured to omit refreshing of the cached memory cells.

22. (canceled)

23. (canceled)

24. (original) A system as recited in claim 19, wherein the use registers comprise bits that each correspond to a row of memory cells.

25. (previously presented) A system comprising:

memory including one or more memory cells;

a memory controller;

an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller based on whether or not virtual-to-physical memory mapping portions are active; and

recent-access flags associated with the one or more memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the system is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval;

wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.

26. (original) A system as recited in claim 25, wherein the memory is dynamically refreshable memory and the memory controller operates the non-allocated memory at reduced power by omitting refreshing of non-allocated memory.

27. (canceled)

28. (previously presented) A system as recited in claim 25, wherein the memory controller is configured to cache at least some of the allocated memory and to omit refreshing of the cached memory.

29. (previously presented) A system as recited in claim 25, further comprising:

a plurality of use bits corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated.

30. (original) A system as recited in claim 25, further comprising a plurality of use bits on the memory controller corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated.

31. (previously presented) A system as recited in claim 25, wherein the memory comprises a plurality of discrete memory devices, the system further comprising a plurality of use bits on the memory devices corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated by configuring the use bits.

32. (currently amended) In a system having dynamically refreshable memory rows, a method of memory power management, comprising:

indicating that memory rows, ~~which have been transferred~~ upon being transferred to a cache, are not in use ~~upon transfer to the cache~~ prior to when the transferred memory rows are written-to in the cache;

keeping track of which memory rows are in use and therefore need refreshing;

periodically refreshing those memory rows that are in use; and

omitting refreshing of memory rows that are not in use.

33. (previously presented) A method as recited in claim 32, further comprising:

determining which rows have been accessed in a manner that refreshed the memory rows during a previous refresh cycle interval, wherein the determining act is performed by utilizing a plurality of recent-access flags associated with each of the memory rows; and

omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory rows during the previous refresh cycle.

34. (previously presented) A method as recited in claim 32, wherein the indicating comprises resetting one or more use registers corresponding to the memory rows that have been transferred to the cache

35. (original) A method as recited in claim 32, wherein keeping track comprises maintaining a plurality of flags corresponding respectively to the memory rows.

36. (canceled)

37. (canceled)

38. (currently amended) A memory controller configured to perform actions comprising:

periodically refreshing memory cells located at one or more memory cell devices;

receiving internal notifications regarding which memory cells are in use based on data stored in a plurality of use registers located on another device including the memory controller; and

omitting refreshing of those memory cells that are not in use.

39. (previously presented) A memory controller as recited in claim 38, the memory controller being configured to perform further actions comprising:

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

40. (previously presented) A memory controller as recited in claim 38, the memory controller being configured to perform further actions comprising:

caching at least some of the memory cells that are in use; and

omitting refreshing of the cached memory cells.

41. (canceled)

42. (canceled)

43. (canceled)

44. (canceled)

45. (canceled)

46. (canceled)

47. (canceled)

48. (canceled)

49. (canceled)

50. (canceled)

51. (canceled)

52. (currently amended) A method for a memory device comprising:

receiving at the memory device memory allocation and de-allocation notifications from an operating system;

periodically refreshing memory cells that are allocated;

omitting refreshing of memory cells that are de-allocated;

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle,

wherein the memory allocation and de-allocation notifications are based on virtual memory mapping portions.

53. (previously presented) A method as recited in claim 52, further comprising:

responsive to the receiving, setting and unsetting use registers corresponding to memory addresses of the memory allocation and de-allocation notifications, respectively

54. (previously presented) A system as recited in claim 19, wherein the use registers are implemented as part of the memory controller.

55. (previously presented) A system as recited in claim 25, wherein the recent-access flags are located on the memory controller, and the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.

56. (previously presented) A system as recited in claim 29, wherein the use bits are implemented as part of the memory cells or as part of the memory controller.

57. (previously presented) A method as recited in claim 34, further comprising:

flushing contents of the cache back to the memory rows; and

setting the one or more use registers corresponding to the memory rows to indicate that the memory rows are in use.

58. (currently amended) A memory controller as recited in claim 39, wherein the keeping track action is performed by utilizing a plurality of recent-access flags located on the other device including the memory controller.

59. (previously presented) A method as recited in claim 53, wherein the setting and unsetting comprises setting and unsetting use registers that are implemented as part of a memory controller.

60. (new) A method as recited in claim 52, wherein the memory device comprises at least one of (i) a memory controller device or (ii) a device having memory cells.

61. (new) A memory device that is capable of receiving memory de-allocation notifications from an operating system; the memory device adapted to omit refreshing of memory cells of memory portions that have been de-allocated responsive to the memory de-allocation notifications.

62. (new) A memory device as recited in claim 61, wherein the memory device comprises at least one of (i) a memory controller device or (ii) a device having the memory cells.

63. (new) A memory device as recited in claim 61, wherein the memory device is further capable of receiving memory allocation notifications from the operating system; the memory device further adapted to periodically refresh memory cells of memory portions that have been allocated responsive to the memory allocation notifications.

64. (new) A memory device as recited in claim 61, wherein the memory de-allocation notifications are based on virtual memory mapping portions.

65. (new) A method for a memory device comprising:

receiving at the memory device memory allocation and de-allocation notifications from an application;

periodically refreshing memory cells that are allocated based on the memory allocation notifications; and

omitting refreshing of memory cells that are de-allocated based on the memory de-allocation notifications.

66. (new) A method as recited in claim 65, wherein the memory device comprises at least one of (i) a memory controller device or (ii) a device having the memory cells.

67. (new) A method as recited in claim 65, further comprising:

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.